IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No.: LOVO-041.DIV

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	06/07/04	Name of Person Making the Deposit:	Judy Davenport	Signature of the Person Making the Deposit:	Judy Davenport

Inventor(s): Pete L. PEGLER

Serial No.: 10/677,570 — Group Art Unit: 2818

Filed: 10/01/03 — Examiner: NHU, David

Confirmation No: 9290

Title: METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF FORMAL DRAWINGS

In response to Drawing Informalities

attached please find:

[X] (a) the formal drawings for this application
Number of Sheets 7

Each sheet of drawing indicates the identifying indicia suggested in § 1.84(c) on the reverse side of the drawing

[ ] (b) a copy of the NOTICE OF INFORMAL DRAWINGS

Please direct all correspondence concerning the above-identified application to the following address:

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Respectfully submitted,

Date: 6/7/2004

By: _____
Anthony C. Murabito
Reg. No. 35,295